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(51) INT CL[6]
H01L 23/52

(52) UK CL (Edition N)
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(56) Documents Cited
EP 0388563 A1

(58) Field of Search
UK CL (Edition N) H1K KHAE
INT CL[6] H01L
Online : WPI

(54) Via-hole and production method of via-hole

(57) In one embodiment, the via hole comprises a sputtered metal layer 8 on which a second metal layer 7, eg of Ni-base alloy, is deposited by electroless-plating. A third metal layer 9, eg of Au, is deposited on the second metal layer by electroplating. In alternative embodiments, (Figs 2 - 8), the first metal layer is deposited by electroless plating, the second metal layer is sputtered on the first layer and the third metal layer is electroplated on the second layer.

Since the inner surface of the hole is completely covered with the sputtered and electroless plated layers, the thick low resistance metal layer 9 can be electroplated over the inner surface of the hole without discontinuity. Further, since the sputtered and electroless plated layers have a good adhesion to the inner surface of the hole, the electroplated layer 9 is formed with a good adhesion.

Fig.1 (d)

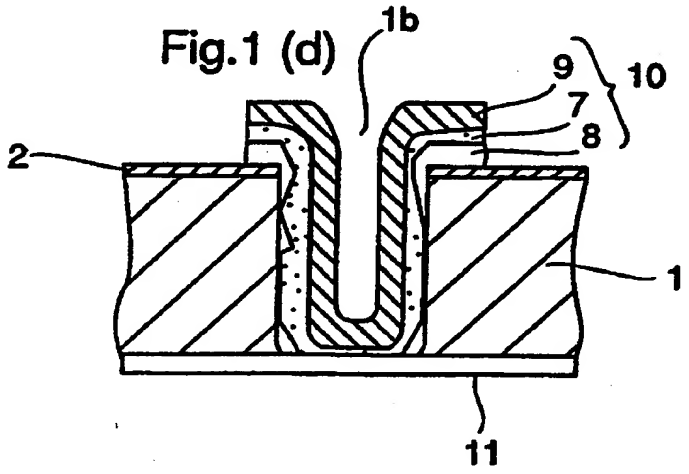

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Fig.1 (a)

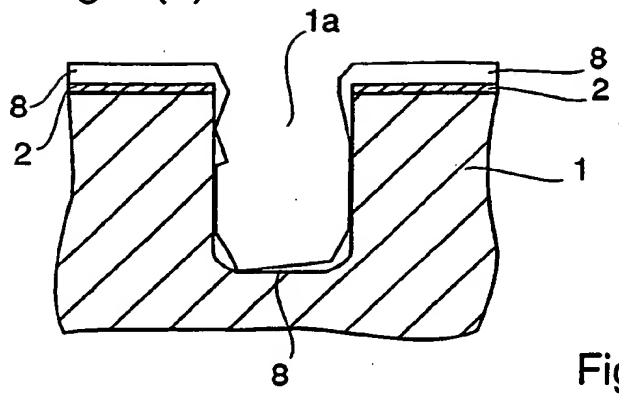


Fig.1 (b)

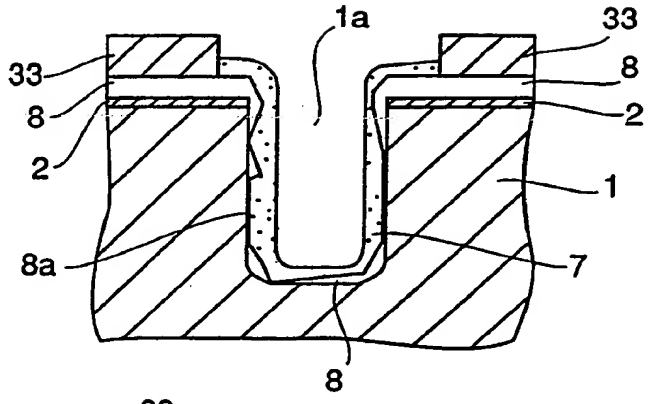


Fig.1 (c)

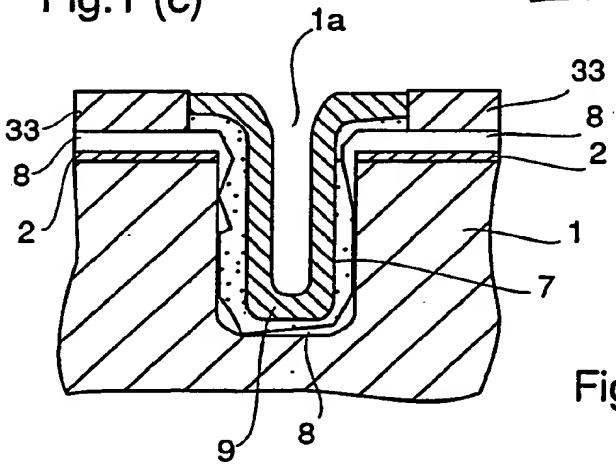


Fig.1 (d)

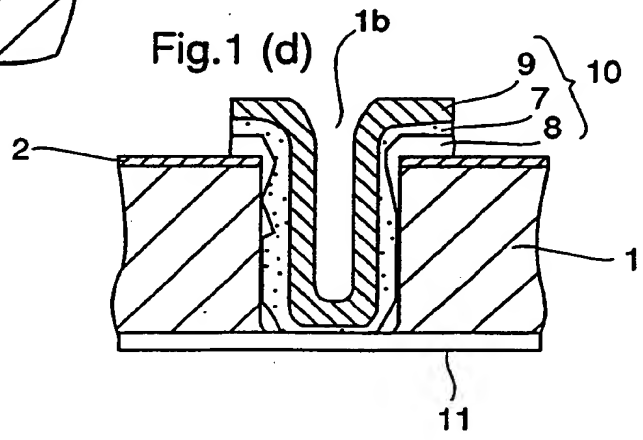


Fig.2 (a)

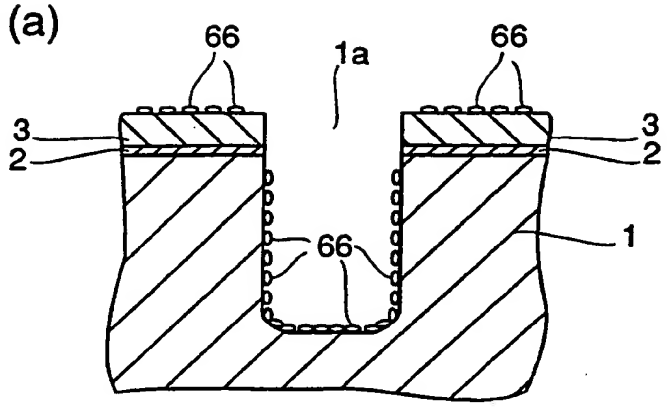


Fig.2 (b)

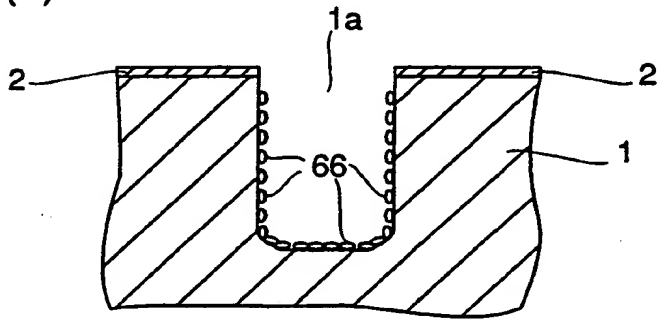
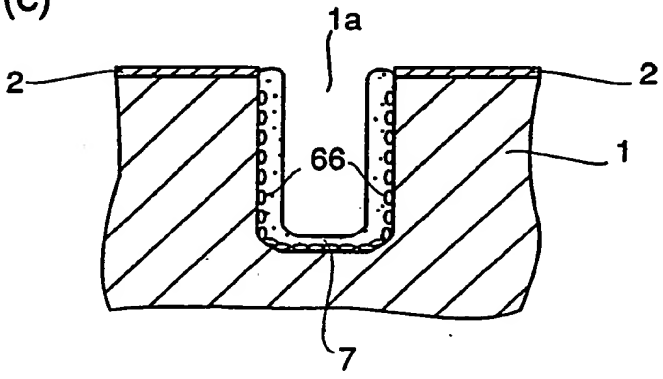


Fig.2 (c)



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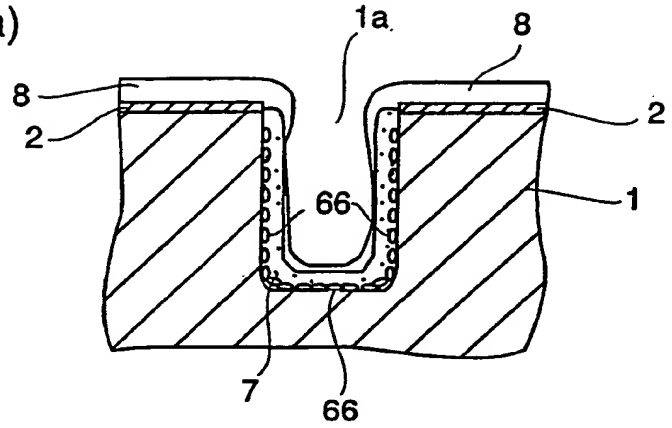


Fig.3 (b)

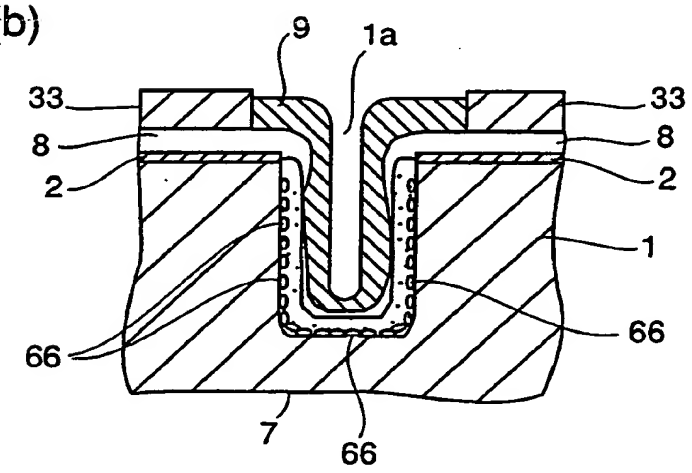
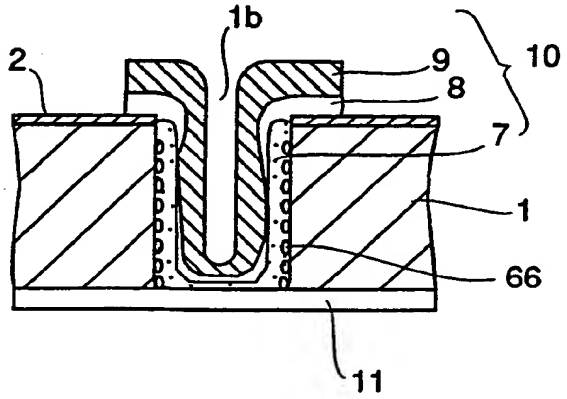


Fig.3 (c)



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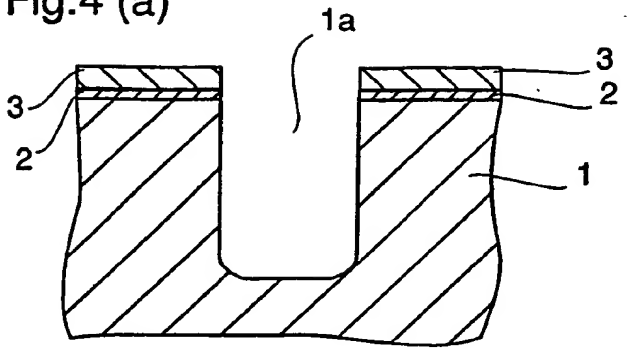


Fig.4 (b)

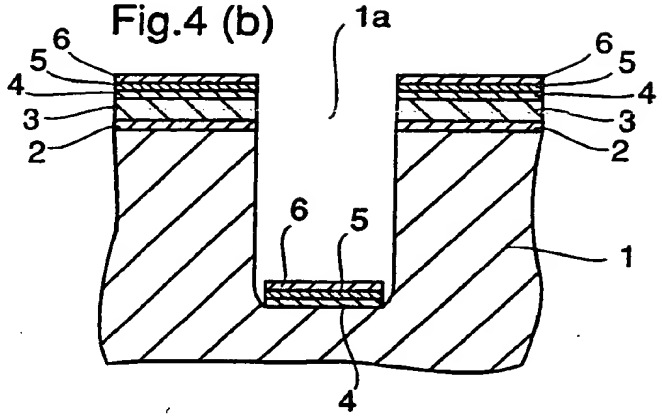


Fig.4 (c)

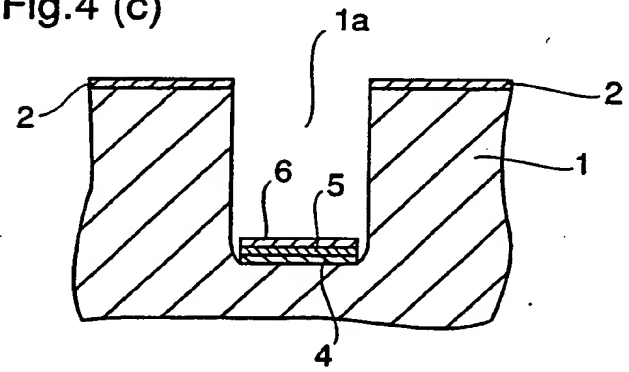
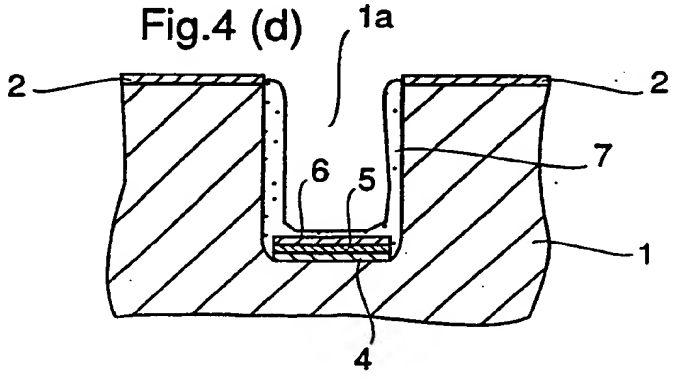


Fig.4 (d)



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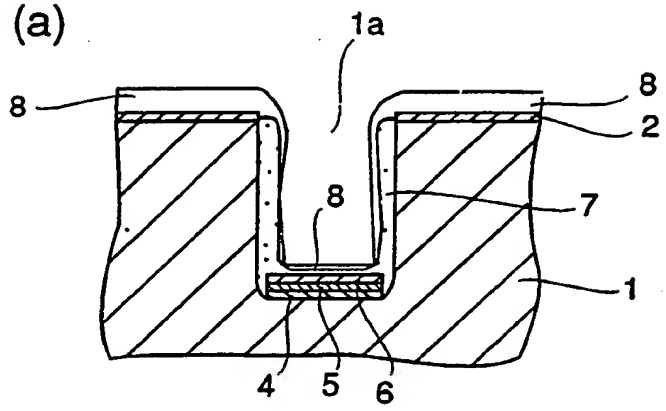


Fig.5 (b)

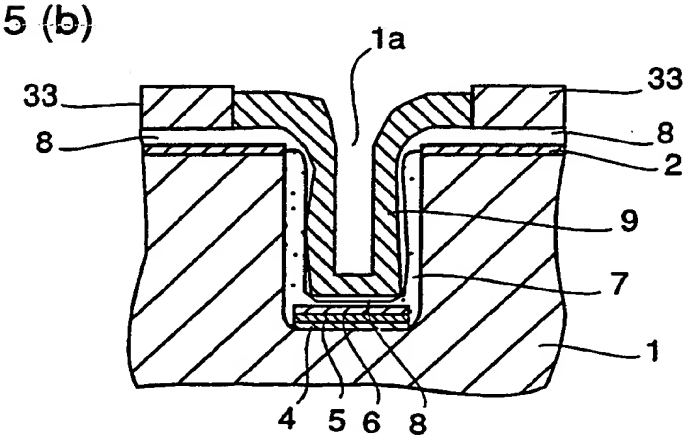
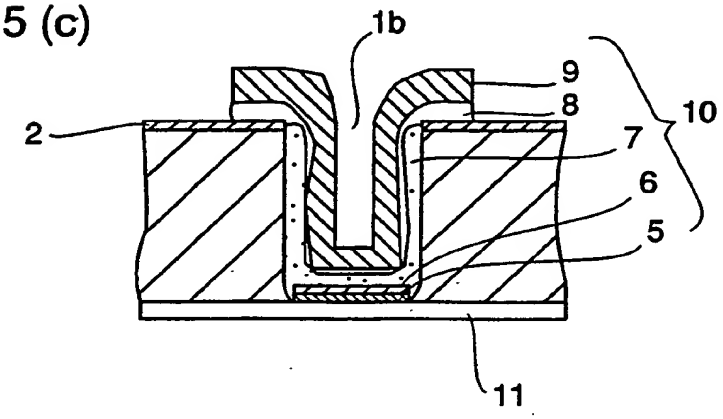


Fig.5 (c)



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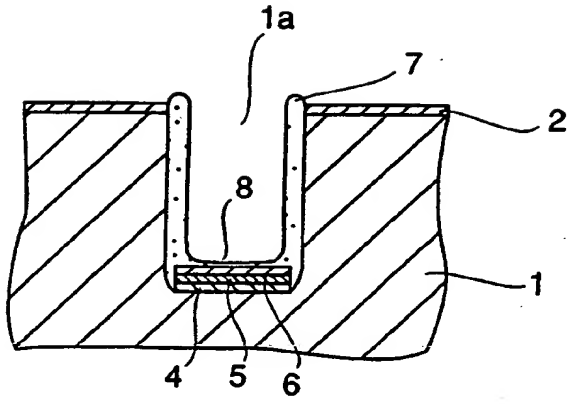
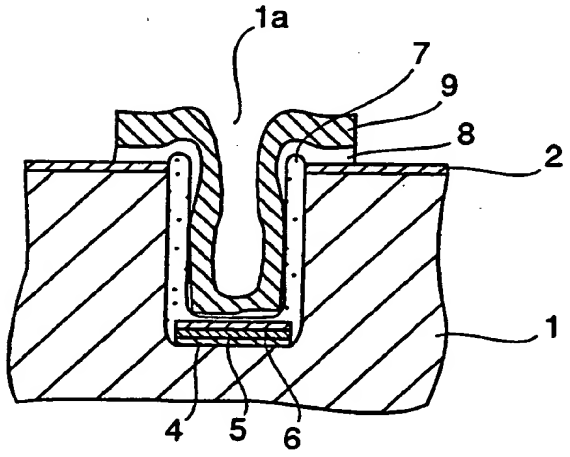


Fig.6 (b)



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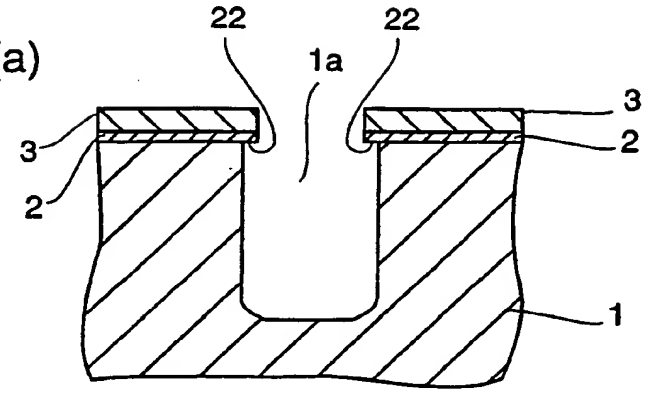


Fig.7 (b)

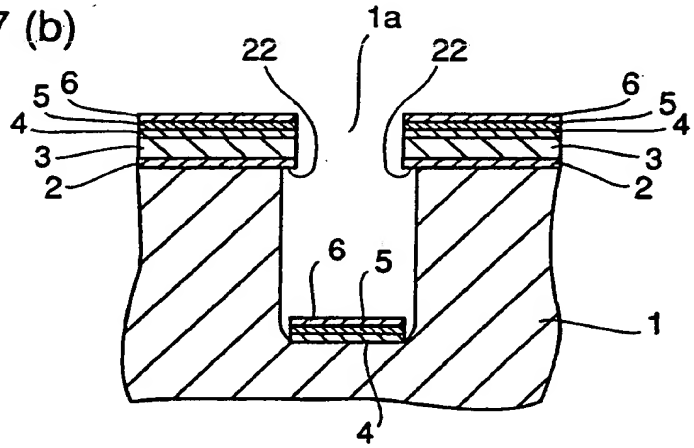


Fig.7 (c)

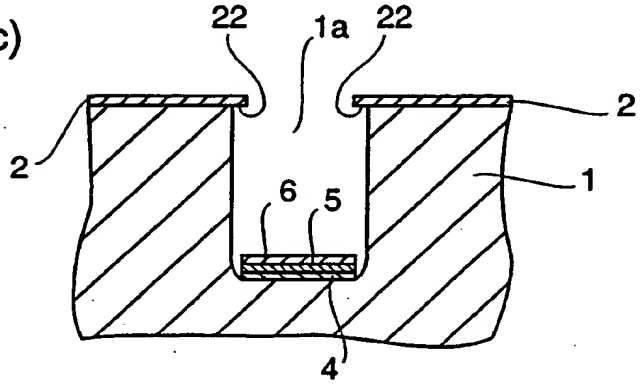


Fig.8 (a)

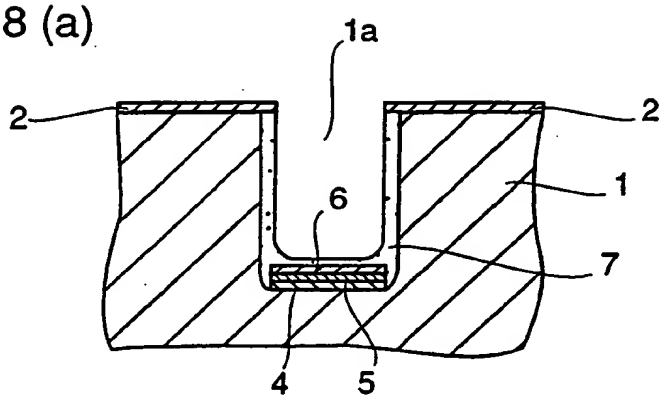


Fig.8 (b)

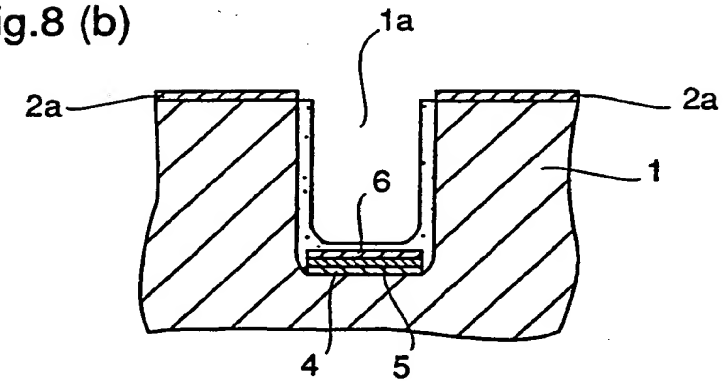
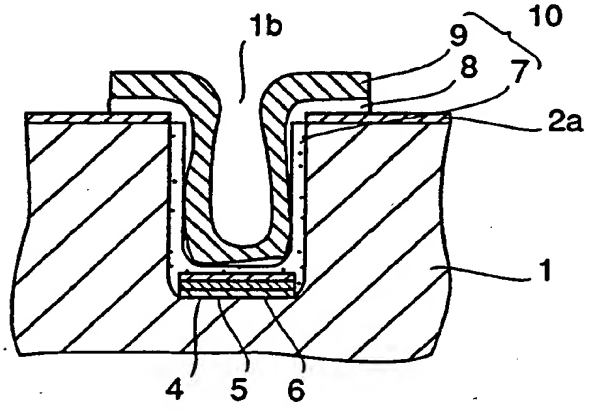


Fig.8 (c)



Prior Art

Fig.9 (a)

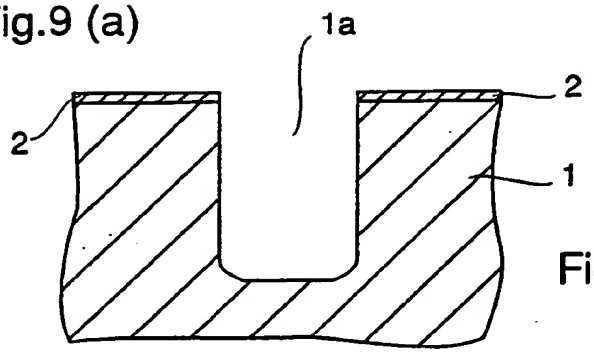


Fig.9 (b)

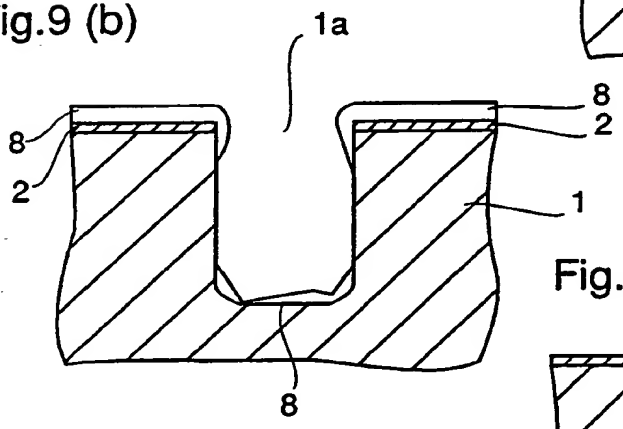


Fig.9 (c)

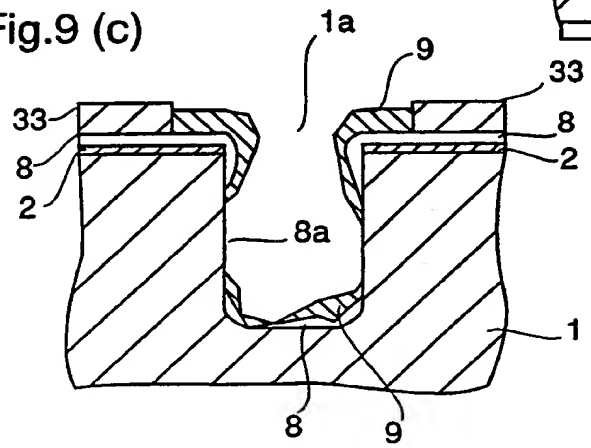


Fig.9 (d)

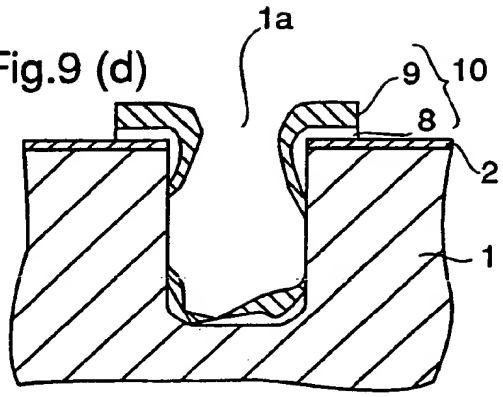
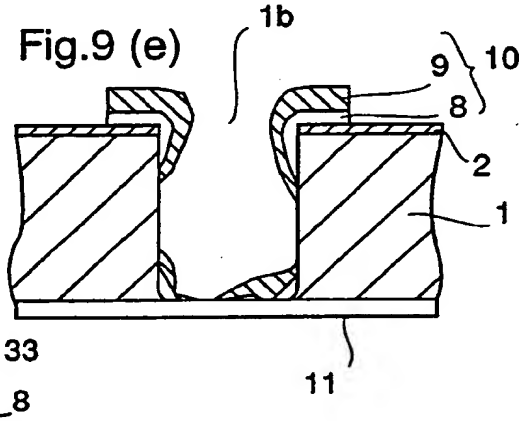


Fig.9 (e)



Prior Art

Fig.10 (a)

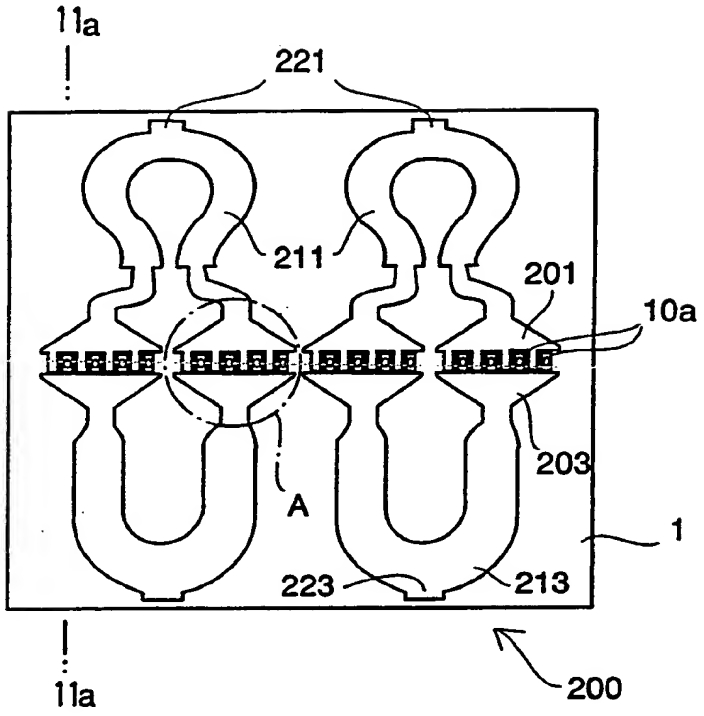
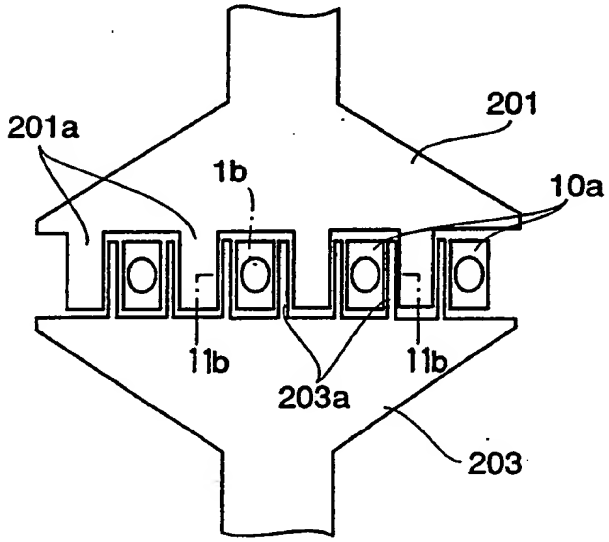


Fig.10 (b)



Prior Art

Fig.11 (a)

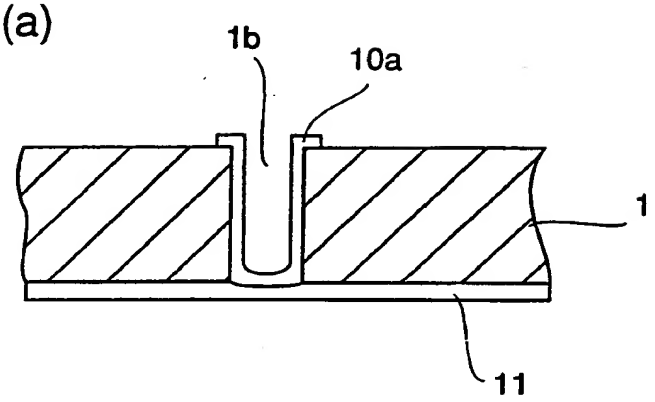
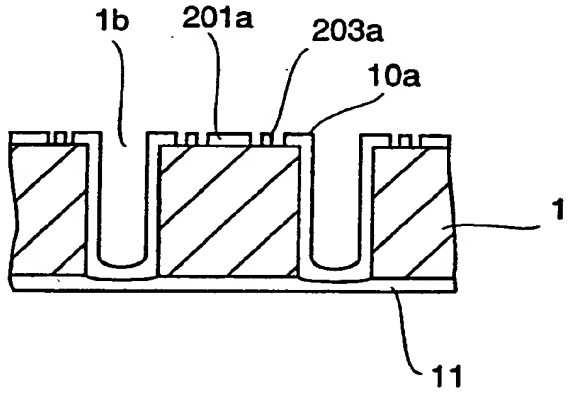


Fig.11 (b)



2285174

VIA-HOLE AND PRODUCTION METHOD OF VIA-HOLE

FIELD OF THE INVENTION

The present invention relates to a via-hole having a high aspect ratio (depth/aperture width), and a method for producing the via-hole.

BACKGROUND OF THE INVENTION

In a conventional semiconductor device, a via-hole is employed as a wiring structure for connecting opposite front and rear surfaces of a semiconductor or insulator substrate through a hole penetrating the substrate.

Figures 9(a)-9(e) are sectional views illustrating process steps of forming a via-hole in a conventional production method of a semiconductor device. In the figures, reference numeral 1 designates a GaAs substrate, numeral 1a designates a bottomed hole formed in the substrate 1, and numeral 1b designates a through-hole penetrating the substrate 1. Reference numeral 2 designates an insulating film comprising SiN or SiON, and numeral 33 designates a photoresist pattern. Reference numeral 8 designates a metal layer formed by depositing Ti and Au in this order using a sputtering technique (hereinafter referred to as a sputtered metal layer), and numeral 8a designates a portion of the inner surface of the hole 1a where the sputtered metal layer 8 is not deposited. Further, reference numeral 9 designates an electroplated Au

layer, numeral 10 designates a wiring pattern, and numeral 11 designates a low resistance metal layer formed over the rear surface of the substrate 1 by vapor deposition or plating.

A description is given of the production process.

Initially, an insulating film 2, such as SiN or SiON, is formed on a GaAs substrate 1, and a photoresist pattern (not shown) is formed on the insulating film 2. Using the photoresist pattern as a mask, the insulating film 2 and the substrate 1 are selectively etched by RIE (Reactive Ion Etching) to form a hole 1a having prescribed width and depth, followed by removal of the photoresist pattern (Figure 9(a)).

Thereafter, the entire surface of the GaAs substrate 1 including the inner surface of the hole 1a is subjected to sputtering of Ti and Au in this order, forming a sputtered metal layer 8 (figure 9(b)). Then, a photoresist pattern 33 is formed on the sputtered metal layer 8 except a region where a wiring pattern is to be produced. Using the photoresist pattern 33 as a mask and the low resistance Au layer of the sputtered metal layer 8 as a feeding layer, an Au layer 9 is selectively electroplated on the exposed part of the sputtered metal layer 8 (figure 9(c)).

After removal of the photoresist pattern 33, portions of the sputtered metal layer 8 exposed by the removal of the

photoresist pattern 33 are selectively removed by ion milling or etching, whereby a wiring pattern 10 is formed from the front surface of the GaAs substrate 1 along the inner wall of the hole 1a (figure 9(d)).

Thereafter, the rear surface of the GaAs substrate 1 is polished until a through-hole 1b penetrating the substrate is formed, i.e., until the wiring pattern 10 is exposed at the rear surface of the substrate. Finally, a low resistance metal layer 11 comprising Au or the like is formed over the rear surface of the GaAs substrate 1 including the exposed wiring pattern 10, preferably by vapor deposition or plating, whereby a via-hole structure shown in figure 9(a) is obtained.

This via-hole is employed as a wiring structure for grounding a microstrip line of a high-frequency semiconductor IC chip or as a wiring structure for grounding a source of an FET.

Figures 10 and 11 illustrate a high-frequency and high-output GaAs MMIC (Monolithic Microwave Integrated Circuit) chip in which via-holes are employed as wirings for grounding source electrodes of FETs. Figure 10(a) is a plan view of the MMIC chip, and figure 10(b) is an enlarged view of a portion A of figure 10(a). Figure 11(a) is a sectional view taken along a line 11a-11a of figure 10(a), and figure 11(b) is a sectional view taken along a line 11b-11b of

figure 10(a).

In the figures, reference numeral 1 designates a GaAs substrate. A plurality of FETs are arranged in a line on the GaAs substrate 1. Gate electrodes 203a of the respective FETs are connected to a common gate electrode 203, and the common gate electrode 203 is connected to a gate bonding pad 223. Drain electrodes of the respective FETs are connected to drain wirings 201a, and the drain wirings 201a are connected to a common drain wiring 201. Further, the common drain wiring 201 is connected to a drain bonding pad 221. Source electrodes of the respective FETs are connected to source grounding wirings 10a. In figures 11(a) and 11(b), the source grounding wiring 10a is connected through the hole 1b to a grounded low resistance metal layer 11a on the rear surface of the substrate 1.

In the above-described production process of a via-hole, after the formation of the sputtered metal layer 8 over the entire surface of the substrate 1 including the inner surface of the hole 1a, the Au layer 9 is selectively electroplated using the sputtered metal layer 8 as a feeding layer. Thereafter, the rear surface of the substrate 1 is polished to expose the wiring pattern 10, and the low resistance metal layer 11 is formed on the rear surface of the substrate 1. In this conventional method, however, when the hole 1a has a high aspect ratio, for example, an

aperture width less than 60 μm and a depth exceeding 100 μm, the sputtered metal layer 8 used as a feeding layer for electroplating is not deposited evenly on the inner surface of the hole 1a. The unevenness of the sputtered metal layer 8 causes an uneven thickness of the Au layer 9 electroplated on the sputtered metal layer 8. When the sputtered metal layer 8 is discontinuous on the inner surface of the hole 1a as shown in figure 9(b), the Au layer 9 electroplated on the sputtered metal layer 8 is also discontinuous between the upper part and the lower part of the hole 1a as shown in figure 9(c). Consequently, the wiring layer on the front surface of the substrate 1, i.e., the electroplated Au layer 9, is not connected to the wiring on the rear surface of the substrate 1, i.e., the low resistance metal layer 11, through the hole 1b.

There is a prior art technique of forming a via-hole wiring, in which an Au layer is plated over the inner surface of the hole of the substrate by electroless plating and, thereafter, the rear surface of the substrate is polished and the rear side wiring is formed. However, since the electroless plating provides a very low growth rate of the Au layer, the thickness of the plated Au layer is very thin. Further, the electroless-plated Au layer has a poor adhesion to the inner surface of the hole. Therefore, in this prior art method, it is impossible to produce a via-

hole with a reliable strength and a low resistance.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a via-hole structure in which a thick metal layer having a low resistance is disposed over an inner surface of a hole of a semiconductor or insulator substrate having a high aspect ratio, and the metal layer is adhered closely to the inner surface of the hole.

It is another object of the present invention to provide a method of producing the via-hole.

Other objects and advantages of the invention will become apparent from the detailed description that follows. The detailed description and specific embodiments described are provided only for illustration since various additions and modifications within the scope of the invention will be apparent to those of skill in the art from the detailed description.

According to a first aspect of the present invention, in a method of producing a via-hole, a hole having a prescribed depth is formed in a prescribed region of a semiconductor substrate, and a base metal layer having a function of a feeding layer for electroplating is formed on the inner surface of the hole by sputtering and electroless plating. Then, a low resistance metal is electroplated using the base metal layer as a feeding layer. Finally, the

rear surface of the substrate is polished, and a wiring layer is formed on the rear surface of the substrate, electrically contacting the electroplated low resistance metal layer. In this method, since the inner surface of the hole is completely covered with the base metal layer formed by sputtering and electroless plating, a thick low resistance metal layer can be electroplated over the inner surface of the hole without discontinuity.

According to a second aspect of the present invention, in a method of producing a via-hole, a hole having a prescribed depth is formed in a prescribed region of a substrate, and a metal layer having a good adhesion to the inner surface of the hole and a function of a feeding layer for electroplating is sputtered over the entire surface of the substrate including the inner surface of the hole. Thereafter, by electroless plating using the sputtered metal layer as a catalyst, a metal layer having a good adhesion to the surface of the sputtered metal layer and the inner surface of the hole is selectively plated on the surface of the sputtered metal layer and on the inner surface of the hole where the sputtered metal layer is absent. Thereafter, a low resistance metal is electroplated using the sputtered metal layer and the electroless-plated metal layer as feeding layers, followed by polishing of the rear surface of the substrate. Finally, a wiring layer is formed on the

rear surface of the substrate, electrically contacting the electroplated low resistance metal layer. In this method, since the inner surface of the hole is completely covered with the sputtered metal layer and the electroless-plated metal layer, a thick low resistance metal layer can be electroplated over the inner surface of the hole without discontinuity. Further, since the sputtered metal layer and the electroless-plated metal layer have a good adhesion to the inner surface of the hole, the electroplated low resistance metal layer is formed with a good adhesion to the inner surface of the hole through the sputtered metal layer and the electroless-plated metal layer.

According to a third aspect of the present invention, in a method of producing a via-hole, a hole having a prescribed depth is formed in a prescribed region of a substrate, and a metal layer having a good adhesion to the inner surface of the hole is selectively plated on the inner surface of the hole by electroless plating. Then, a metal layer having a good adhesion to the surfaces of the substrate and the electroless-plated metal layer and having a function of a feeding layer is sputtered over these surfaces. Thereafter, a low resistance metal is electroplated using the sputtered metal layer and the electroless-plated metal layer as feeding layers, followed by polishing of the rear surface of the substrate. Finally,

a wiring layer is formed on the rear surface of the substrate, electrically contacting the electroplated low resistance metal layer. In this method, since the inner surface of the hole is completely covered with the sputtered metal layer and the electroless-plated metal layer, a thick low resistance metal layer can be electroplated over the inner surface of the hole without discontinuity. Further, since the sputtered metal layer and the electroless-plated metal layer have a good adhesion to the inner surface of the hole, the electroplated low resistance metal layer is formed with a good adhesion to the inner surface of the hole through the sputtered metal layer and the electroless-plated metal layer.

According to a fourth aspect of the present invention, in the above-described method of producing a via-hole, the electroless-plated metal layer is formed on the inner surface of the hole so that it does not have a portion protruding from the hole over the front surface of the substrate. Therefore, the sputtered metal layer and the electroplated metal layer formed on the electroless-plated metal layer do not swell at the periphery of the opening of the hole, so that portions of these layers on the front surface of the substrate are made flat.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1(a)-1(d) are sectional views illustrating

process steps in a method of producing a via-hole of a semiconductor device in accordance with a first embodiment of the present invention.

Figures 2(a)-2(c) and 3(a)-3(c) are sectional views illustrating process steps in a method of producing a via-hole of a semiconductor device in accordance with a second embodiment of the present invention.

Figures 4(a)-4(d) and 5(a)-5(c) are sectional views illustrating process steps in a method of producing a via-hole of a semiconductor device in accordance with a third embodiment of the present invention.

Figures 6(a) and 6(b) are sectional views for explaining a problem in the production process according to the second and third embodiments of the invention.

Figures 7(a)-7(c) and 8(a)-8(c) are sectional views illustrating process steps in a method of producing a via-hole of a semiconductor device in accordance with a fourth embodiment of the present invention.

Figures 9(a)-9(e) are sectional views illustrating process steps in a method of producing a via-hole of a semiconductor device according to the prior art.

Figures 10(a) and 10(b) are diagrams for explaining a conventional high-frequency and high-output MMIC, in which figure 10(a) is a plan view of the MMIC, and figure 10(b) is an enlarged view of a portion A of figure 10(a).

Figure 11(a) is a sectional view taken along a line 11a-11a of figure 10(a), and figure 11(b) is a sectional view taken along a line 11b-11b of figure 10(a).

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[Embodiment 1]

Figures 1(a)-1(d) are sectional views illustrating process steps in a method of producing a via-hole of a semiconductor device in accordance with a first embodiment of the present invention. In the figures, the same reference numerals as in figures 9(a)-9(e) designate the same or corresponding parts. Reference numeral 7 designates an Ni base alloy layer comprising, for example, Ni-P, Ni-B, or Ni-B-W, formed by electroless-plating (hereinafter referred to as an electroless-plated Ni base alloy layer).

A description is given of the production process.

Initially, an insulating film 2, such as SiN or SiON, is formed on the surface of the GaAs substrate 1, and a photoresist pattern (not shown) is formed on the insulating film 2. Using the photoresist film 2 as a mask, the insulating film 2 and the GaAs substrate 1 are selectively etched by RIE to form a hole 1a having a depth of 100 - 120 μm and an aperture width of 50 - 60 μm, followed by removal of the photoresist pattern.

Thereafter, a first metal layer comprising Ti, Cr, or Ni and having a thickness less than 500 Å and a second metal

layer comprising a low resistance metal, such as Au, and having a thickness of about 2000 Å are successively deposited over the entire surface of the GaAs substrate 1 including the inner surface of the hole 1a using a sputtering technique, whereby a sputtered metal layer 8 is formed (figure 1(a)). The first metal layer comprising Ti, Cr, or Ni has a good adhesion to the inner surface of the hole 1a of the GaAs substrate 1. Then, a photoresist pattern 33 is formed on the sputtered metal layer 8 except a region where a wiring pattern is to be formed. Using the photoresist pattern 33 as a mask and the sputtered metal layer 8 as a catalyst, an Ni base alloy layer 7 about 5000 Å thick is selectively formed on the unmasked portion of the sputtered metal layer 8 and on the inner surface of the hole 1a where the sputtered metal layer 8 is absent, by electroless plating (figure 1(b)). The electroless-plated Ni base alloy layer 7 has a good adhesion to the surface of the sputtered metal layer 8 and the inner surface of the hole 1a.

Thereafter, using the low resistance Au layer included in the sputtered metal layer 8 and the electroless-plated Ni base alloy layer 7 as feeding layers, an Au layer 9 having a thickness exceeding 3 μm is formed on the electroless-plated Ni base alloy layer 7 by electroplating (figure 1(c)).

After removal of the photoresist pattern 33, portions

of the sputtered metal layer 8 exposed by the removal of the photoresist pattern 33 are selectively removed by ion milling or etching, whereby a wiring pattern 10 is formed from the front surface of the GaAs substrate 1 over the inner surface of the hole 1a of the substrate 1. Thereafter, the rear surface of the GaAs substrate 1 is polished until the wiring pattern 10 is exposed, i.e., until a through-hole 1b penetrating the substrate 1 is formed. Finally, an Au layer 11 is formed over the rear surface of the GaAs substrate 1 including the exposed surface of the wiring pattern 10, preferably by vapor deposition or plating, resulting in a via-hole structure in which the wiring pattern 10 is connected to the rear side wiring 11 via the through-hole 1b (figure 1(d)). Since the first metal layer comprising Ti, Cr, or Ni of the sputtered metal layer 8 has a high resistance, it is desired that the polishing of the GaAs substrate 1 is carried out until the high resistance first metal layer is completely removed and the second metal layer, i.e., the low resistance Au layer, is exposed.

In this first embodiment of the present invention, after formation of the sputtered metal layer 8 on the inner surface of the hole 1a of the GaAs substrate 1, the electroless-plated Ni base alloy layer 7 is formed on the sputtered metal layer 8 and on portions of the inner surface

of the hole 1a where the sputtered metal layer 8 is absent. Thereafter, using the sputtered metal layer 8 and the electroless-plated Ni base alloy layer 7 as feeding layers, the Au layer 9 is electroplated. Therefore, a thick electroplated Au layer 9 exceeding 3 μm is evenly formed over the inner surface of the hole 1a without discontinuity. In addition, the first metal layer comprising Ti, Cr, or Ni included in the sputtered metal layer 8 adheres closely to the inner surface of the hole 1a with a good adhesion, and the electroless-plated Ni base alloy layer 7 adheres closely to the sputtered metal layer 8 and the inner surface of the hole 1a with a good adhesion. Therefore, the electroplated Au layer 9 is formed with a good adhesion to the inner surface of the hole 1a through the sputtered metal layer 8 and the electroless-plated Ni base layer 7. After the formation of the wiring pattern 10 comprising the above-described layers 7, 8, and 9, the rear surface of the GaAs substrate 1 is polished to expose the wiring pattern 10, and the Au layer 11 is formed on the rear surface of the substrate. In the via-hole structure produced in this way, the wiring on the front surface of the substrate 1, i.e., the wiring pattern 10 including the electroplated Au layer 9, is connected to the wiring on the rear surface of the substrate, i.e., the Au layer 11, through the through-hole 1b, with high reliability. Further, the strength of the

via-hole is improved.

[Embodiment 2]

Figures 2(a)-2(c) and 3(a)-3(c) are sectional views illustrating process steps in a method of producing a via-hole of a semiconductor device in accordance with a second embodiment of the present invention. In figures, the same reference numerals as in figures 1(a)-1(d) designate the same or corresponding parts. Reference numeral 66 designates Pd nuclei serving as a catalyst of electroless plating.

A description is given of the production process.

Initially, an insulating film 2 comprising SiN or SiON is formed on the surface of the GaAs substrate 1, and a photoresist pattern 3 is formed on the insulating film 2. Using the photoresist pattern 3 as a mask, the insulating film 2 and the GaAs substrate 1 are etched by RIE to form a hole 1a having a depth of 100 - 120 μm and an aperture width of 50 - 60 μm. Thereafter, using the photoresist pattern 3 as a mask, a Pd activated solution, for example, a mixture of $PdCl_2$ and HCl, is applied to the inner surface of the hole 1a, whereby Pd nuclei 66 are deposited on the inner surface of the hole 1a (figure 2(a)).

After removal of the photoresist pattern 3 (figure 2(b)), by electroless plating using the insulating film 2 as a mask and the Pd nuclei 66 as a catalyst, an Ni base alloy

layer 7, such as Ni-P, Ni-B, or Ni-B-W, is selectively formed on the inner surface of the hole 1a to a thickness of about 5000 Å (figure 2(c)). The electroless-plated Ni base alloy layer 7 adheres closely to the surface of the hole 1a with a good adhesion.

Thereafter, a first metal layer comprising Ti, Cr, or Ni and having a thickness less than 500 Å and a second metal layer comprising a low resistance metal, such as Au, and having a thickness of about 2000 Å are successively sputtered on the surface of the insulating film 2 and on the surface of the electroless-plated Ni base alloy layer 7 in the hole 1a, resulting in a sputtered metal layer 8 (figure 3(a)).

In the step of figure 3(b), a photoresist pattern 33 is formed on the sputtered metal layer 8 except a region where a wiring pattern is to be formed. Using the photoresist pattern 33 as a mask, an Au layer 9 having a thickness of 3 μm or more is selectively electroplated on the sputtered metal layer 8 and on the electroless-plated Ni base alloy layer 7. The sputtered metal layer 8 and the Ni base alloy layer 7 serve as feeding layers for the electroplating.

After removal of the photoresist pattern 33, portions of the sputtered metal layer 8 exposed by the removal of the photoresist pattern 33 are selectively removed by ion milling or etching, whereby a wiring pattern 10 is formed

from the front surface of the GaAs substrate 1 over the inner surface of the hole 1a of the substrate 1. Thereafter, the rear surface of the GaAs substrate 1 is polished until the wiring pattern 10 is exposed at the rear surface, i.e., until a through-hole 1b penetrating the substrate 1 is formed. Finally, an Au layer 11 is formed on the rear surface of the GaAs substrate 1 including the exposed surface of the wiring pattern 10 by vapor deposition or plating, resulting in a via-hole structure in which the wiring pattern 10 is connected to the rear side Au wiring 11 via the through-hole 1b (figure 3(c)).

In this second embodiment of the present invention, after the selective electroless plating of the Ni base alloy layer 7 on the inner surface of the hole 1a of the GaAs substrate 1, the sputtered metal layer 8 having a function of a feeding layer for electroplating is formed on the front surface of the GaAs substrate 1 and on the surface of the electroless-plated Ni base alloy layer 7. Thereafter, the Au layer 9 is electroplated on the sputtered metal layer 8 and on the electroless-plated Ni base alloy layer 7 using these layers as feeding layers. Therefore, a thick electroplated Au layer exceeding 3 μm can be formed without discontinuity. In addition, the electroless-plated Ni base alloy layer 7 comprising Ni-P, Ni-B, Ni-B-W, or the like adheres closely to the inner surface of the hole 1a of the

GaAs substrate 1 with a good adhesion, and the first metal layer comprising Ti, Cr, or Ni included in the sputtered metal layer 8 adheres closely to the electroless-plated Ni base alloy layer 7 and the insulating film 2 with a good adhesion. Therefore, the electroplated Au layer 9 is formed with a good adhesion to the inner surface of the hole 1a through the sputtered metal layer 8 and the electroless-plated Ni base layer 7. After the formation of the wiring pattern 10 comprising the above-described layers 7, 8, and 9, the rear surface of the GaAs substrate 1 is polished to expose the wiring pattern 10, and the Au layer 11 is formed on the rear surface of the substrate. In the via-hole structure produced in this way, the wiring on the front surface of the substrate 1, i.e., the wiring pattern 10 including the electroplated Au layer 9, is connected to the wiring on the rear surface of the substrate, i.e., the Au layer 11, via the through-hole 1b, with high reliability. Further, the strength of the via-hole is improved.

[Embodiment 3]

Figures 4(a)-4(d) and 5(a)-5(c) are sectional views illustrating process steps of producing a via-hole of a semiconductor device in accordance with a third embodiment of the present invention. In these figures, the same reference numerals as in figures 1(a)-1(d) designate the same or corresponding parts. Reference numeral 4 designates

a metal layer comprising one selected from Ti, Cr, and Ni, numeral 5 designates an Au layer, and numeral 6 designates a Pd layer. These layers 4, 5, and 6 are formed by vapor deposition.

A description is given of the production process.

Initially, an insulating film 2, such as SiN or SiON, is formed on the surface of the GaAs substrate 1, and a photoresist pattern 3 is formed on the insulating film 2. Using the photoresist pattern 3 as a mask, the insulating film 2 and the GaAs substrate 1 are selectively etched by RIE to form a hole 1a having a depth of 100 - 120 μm and an aperture width of 50 - 60 μm (figure 4(a)).

Using the photoresist pattern 3 as a mask, a metal layer 4 comprising Ti, Cr, or Ni and having a thickness less than 500 Å, an Au layer 5 having a thickness less than 500 Å, and a Pd layer 6 having a thickness less than 500 Å are successively deposited on the bottom of the hole 1a by vapor deposition (figure 4(b)). The metal layer 4 comprising Ti, Cr, or Ni adheres closely to the bottom of the hole 1a. The Pd layer 6 serves as a catalyst in the subsequent electroless plating process. The Au layer 5 interposed between the metal layer 4 and the Pd layer 6 serves as a buffer layer that prevents separation of the Pd layer 6 from the metal layer 4 due to the difference in linear expansion coefficients between these layers 4 and 6.

After removal of the photoresist pattern 3 (figure 4(c)), using the insulating film 2 as a mask and the Pd layer 6 as a catalyst, an Ni base alloy layer 7 about 5000 Å thick is formed on the inner surface of the hole 1a by electroless plating (figure 4(d)).

Thereafter, a first metal layer comprising Ti, Cr, or Ni and having a thickness less than 500 Å and a second metal layer comprising a low resistance metal, such as Au, and having a thickness of about 2000 Å are successively sputtered on the surface of the insulating film 2 and on the surface of the electroless-plated Ni base alloy layer 7 in the hole 1a, resulting in a sputtered metal layer 8 (figure 5(a)).

In the step of figure 5(b), a photoresist pattern 33 is formed on the sputtered metal layer 8 except a region where a wiring pattern is to be formed. Using the photoresist pattern 33 as a mask, an Au layer 9 having a thickness exceeding 3 μm is selectively electroplated on the sputtered metal layer 8 and on the electroless-plated Ni base alloy layer 7. The sputtered metal layer 8 and the electroless-plated Ni base alloy layer 7 serve as feeding layers in the electroplating process.

After removal of the photoresist pattern 33, portions of the sputtered metal layer 8 exposed by the removal of the photoresist pattern 33 are selectively removed by ion

milling or etching, whereby a wiring pattern 10 is formed from the front surface of the GaAs substrate 1 over the inner surface of the hole 1a. Thereafter, the rear surface of the GaAs substrate 1 is polished until the wiring pattern 10 is exposed at the rear surface, i.e., until a through-hole 1b penetrating the substrate 1 is formed. Finally, an Au layer 11 is formed over the rear surface of the GaAs substrate 1 including the exposed surface of the wiring pattern 10 by vapor deposition or plating, resulting in a via-hole structure in which the wiring pattern 10 is connected to the rear side Au wiring 11 via the through-hole 1b (figure 5(c)). Since the metal layer 4 comprising Ti, Cr, or Ni has a high resistance, it is desired that the polishing of the substrate 1 is carried out until the high resistance metal layer 4 is completely removed and the low resistance Au layer 5 is exposed.

Also in this third embodiment of the invention, the same effects as described in the second embodiment are achieved. In addition, since the vapor-deposited Pd layer 6 is used as a catalyst for the electroless plating of the Ni base alloy layer 7, the process of immersing the substrate 1 in a Pd activated solution to deposit Pd nuclei as in the second embodiment can be dispensed with.

In the production of the via-hole structure according to the second or third embodiment of the invention, the

electroless-plated Ni base alloy layer 7 sometimes protrudes over the periphery of the opening of the hole 1a as shown in figure 6(a). In this case, as shown in figure 6(b), the protruding portion of the Ni base alloy layer 7 causes an uneven surface of the electroplated Au layer 9 at the periphery of the opening of the hole 1a. The uneven portion of the Au layer 9 is an obstacle to a stable wire-bonding on the Au layer 9. This problem is solved in a fourth embodiment of the present invention described hereinafter.

[Embodiment 4]

Figures 7(a)-7(c) and 8(a)-8(c) are sectional views illustrating process steps of producing a via-hole of a semiconductor device according to the fourth embodiment of the present invention. In the figures, the same reference numerals as in figures 1(a)-1(d) designate the same or corresponding parts. Reference numeral 2a designates an insulating film, and numeral 22 designates an overhanging portion of the insulating film 2.

A description is given of the production process.

Initially, an insulating film 2, such as SiN or SiON, is formed on the surface of the GaAs substrate 1, and a photoresist pattern 3 is formed on the insulating film 2. Using the photoresist pattern 3 as a mask, the insulating film 2 and the GaAs substrate 1 are selectively etched by RIE to form a hole having prescribed depth and width. Then,

the inner surface of the hole 1a is subjected to isotropic chemical etching that over-etches the side wall of the hole, whereby a hole 1a having a depth of 100 - 120 μm and an aperture width of 50 - 60 μm is formed (figure 7(a)). The insulating film 2 has a portion 22 overhanging the hole 1a.

As in the above-described third embodiment, using the photoresist pattern 3 as a mask, a metal layer comprising one selected from Ti, Cr, and Ni and having a thickness less than 500 Å, an Au layer 5 having a thickness less than 500 Å, and a Pd layer 6 having a thickness less than 500 Å are successively vapor-deposited on the bottom of the via-hole 1a (figure 7(b)).

After removal of the photoresist pattern 3 (figure 7(c)), using the insulating film 2 as a mask and the vapor-deposited Pd layer 6 as a catalyst, an Ni base alloy layer 7 about 5000 Å thick is formed on the inner surface of the hole 1a by electroless plating (figure 8(a)). In the electroless plating, the overhanging portion 22 of the insulating film 2 prevents the plated Ni base alloy layer 7 from protruding over the front surface of the GaAs substrate 1.

The overhanging portion 22 of the insulating film 2 is removed by ion milling or selective etching (figure 8(b)). Thereafter, as illustrated in figure 8(c), the sputtered metal layer 8 and the electroplated Au layer 9 are

selectively formed in the same process as described with respect to figures 5(a) and 5(b). Finally, as illustrated in figure 5(c), the rear surface of the GaAs substrate 1 is polished to expose the wiring pattern 10, and the Au layer 11 is formed over the rear surface of the substrate 1, whereby a via-hole structure in which the wiring pattern 10 is connected to the rear side Au wiring 11 via the through-hole 1b is produced.

Also in this fourth embodiment of the invention, the same effects as described in the third embodiment are achieved. Further, since the unwanted protrusion of the electroless-plated Ni base alloy layer 7 from the periphery of the opening of the hole 1a is avoided, the electroplated Au layer 9 on the front surface of the GaAs substrate 1 has an even surface that facilitates the subsequent wire-bonding of the Au layer 9.

In the above-described first to fourth embodiments, after the formation of the electroless-plated Ni base alloy layer 7, the surface of the electroless-plated Ni base alloy layer 7 may be substituted by a substitution type electroless plating of Au. In this case, the adhesion between the electroless-plated Ni base alloy layer 7 and the electroplated Au layer 9 is improved.

Although in the above-described first to fourth embodiments the insulating film 2 is used as a mask for the

electroless plating of the Ni base alloy layer 7, when another metal pattern is exposed in a region of the substrate other than the region shown in the figures, a photoresist pattern masking this metal pattern is formed before the formation of the electroless-plated Ni base alloy layer 7.

While in the above-described first to fourth embodiments the electroless-plated metal layer 7 comprises Ni base alloy, the electroless-plated metal layer 7 may comprise other metals so far as the metal has a good adhesion to the surface to which it is plated.

While in the above-described first to fourth embodiments Au is employed as a low resistance metal, other low resistance metals, such as Ag or Cu, may be employed.

In the foregoing description, emphasis has been placed upon a via-hole structure of a semiconductor device employing a GaAs substrate. However, the structure and the production process of the via-hole according to the present invention may be applied to other semiconductor devices including substrates of other semiconductor materials or insulators, such as sapphire, or devices other than semiconductor devices and including insulator substrates.

Claims

1. A via-hole comprising:

a substrate having a surface;

a through-hole penetrating the substrate and having an inner surface;

a sputtered metal layer disposed on part of the surface of the substrate and on the inner surface of the through-hole ;

an electroless-plated metal layer disposed on the sputtered metal layer and the inner surface of the through-hole ; and

an electroplated metal layer disposed on the electroless-plated metal layer .

2. The via-hole of claim 1 wherein said through-hole has a depth and an aperture width in an aspect ratio (depth/aperture width) larger than 5/3.

3. The via-hole of claim 1 wherein said sputtered metal layer comprises a first metal layer comprising one selected from Ti, Cr, and Ni and having a good adhesion to the inner surface of the through-hole , and a second metal layer having a low resistance disposed on the first metal layer.

4. The via-hole of claim 1 wherein said electroless-plated metal layer is an electroless-plated Ni base alloy layer.

5. The via-hole of claim 1 wherein said electroplated metal layer is an electroplated Au layer.

6. A via-hole comprising:

a substrate having a surface;

a through-hole penetrating the substrate and having an inner surface;

an electroless-plated metal layer disposed on the inner surface of the through-hole ;

a sputtered metal layer disposed on part of the surface of the substrate and on the electroless-plated metal layer ; and

an electroplated metal layer disposed on the electroless-plated metal layer and on the sputtered metal layer .

7. The via-hole of claim 6 wherein said through-hole has a depth and an aperture width in an aspect ratio (depth/aperture width) larger than 5/3.

8. The via-hole of claim 6 wherein said sputtered

metal layer comprises a first metal layer comprising one selected from Ti, Cr, and Ni and having a good adhesion to the inner surface of the through-hole , and a second metal layer having a low resistance and disposed on the first metal layer.

9. The via-hole of claim 6 wherein said electroless-plated metal layer is an electroless-plated Ni base alloy layer.

10. The via-hole of claim 6 wherein said electroplated metal layer is an electroplated Au layer.

11. A method of producing a via-hole comprising:

forming a hole in a prescribed region of a substrate having opposite front and rear surfaces, said hole having a prescribed depth from the front surface of the substrate and an inner surface;

sputtering a metal layer on the inner surface of the hole ;

plating a metal layer on the inner surface of the hole and on the sputtered metal layer by electroless plating; and

electroplating a low resistance metal layer on

the electroless-plated metal layer .

12. The method of claim 11 further comprising:

after formation of the electroplated low resistance metal layer , polishing the rear surface of the substrate until the hole penetrates through the substrate ; and

forming a low resistance metal layer over the rear surface of the substrate , electrically contacting the electroplated metal layer .

13. A method of producing a via-hole comprising:

forming a hole in a prescribed region of a substrate having opposite front and rear surfaces, said hole having a prescribed depth from the front surface of the substrate and an inner surface;

sputtering a metal layer on part of the front surface of the substrate and on the inner surface of the hole ;

selectively plating a metal layer on the inner surface of the hole where the sputtered metal layer is absent and on a portion of the sputtered metal layer to be a wiring layer, by electroless plating using the sputtered metal layer as a catalyst; and

electroplating a low resistance metal layer on

the electroless-plated metal layer using the sputtered metal layer and the electroless-plated metal layer as feeding layers.

14. The method of claim 13 wherein said hole has a depth and an aperture width in an aspect ratio (depth/aperture width) larger than 5/3.

15. The method of claim 13 wherein said sputtered metal layer is formed by sputtering a first metal having a good adhesion to the inner surface of the hole on the inner surface of the hole and then sputtering a second metal having a low resistance on the sputtered first metal.

16. The method of claim 15 wherein the first metal is one selected from Ti, Cr, and Ni, and the second metal is Au.

17. The method of claim 13 wherein said electroless-plated metal layer is an electroless-plated Ni base alloy layer.

18. The method of claim 13 wherein said electroplated metal layer is an electroplated Au layer.

19. The method of claim 17 further including substituting the surface of the electroplated Ni base alloy layer by a substitution type electroless plating of Au.

20. The method of claim 13 further comprising:

after formation of the electroplated low resistance metal layer, polishing the rear surface of the substrate until the hole penetrates through the substrate; and

forming a low resistance metal layer over the rear surface of the substrate, electrically contacting the electroplated metal layer.

21. A method of producing a via-hole and comprising:

forming a hole in a prescribed region of a substrate having opposite front and rear surfaces, said hole having a prescribed depth from the front surface of the substrate and an inner surface;

plating a metal layer on the inner surface of the hole by electroless plating;

sputtering a metal layer on the front surface of the substrate and on the electroless-plated metal layer; and

electroplating a low resistance metal layer on

the sputtered metal layer and on the electroless-plated metal layer using the sputtered metal layer and the electroless-plated metal layer as feeding layers.

22. The method of claim 21 wherein said hole has a depth and an aperture width in an aspect ratio (depth/aperture width) larger than 5/3.

23. The method of claim 21 wherein said electroless-plated metal layer is an electroless-plated Ni base alloy layer.

24. The method of claim 21 wherein said electroless-plated metal layer is formed by electroless-plating an Ni base alloy layer on the inner surface of the hole using, as a catalyst, a Pd layer selectively vapor-deposited at the bottom of the hole.

25. The method of claim 21 wherein said sputtered metal layer is formed by sputtering a first metal having a good adhesion to the surface of the substrate and to the surface of the electroless-plated metal layer and then sputtering a second metal having a low resistance on the sputtered first metal.

26. The method of claim 21 wherein said electroplated metal layer is an electroplated Au layer.

27. The method of claim 23 further including substituting the surface of the electroplated Ni base alloy layer by a substitution type electroless plating of Au.

28. The method of claim 24 further including substituting the surface of the electroplated Ni base alloy layer by a substitution type electroless plating of Au.

29. The method of claim 25 wherein the first metal is one selected from Ti, Cr, and Ni, and the second metal is Au.

30. The method of claim 21 further including:

after formation of the electroplated low resistance metal layer, polishing the rear surface of the substrate until the hole penetrates through the substrate; and

forming a low resistance metal layer over the rear surface of the substrate, electrically contacting the electroplated metal layer.

31. A method of producing a via-hole

comprising:

preparing a substrate having opposite front and rear surfaces;

forming an insulating film on the front surface of the substrate ;

selectively etching portions of the insulating film and the substrate by anisotropic etching, thereby forming an opening in a prescribed region of the insulating film and a hole in the substrate opposite the opening of the insulating film , said hole having a prescribed depth from the front surface of the substrate ;

selectively etching the substrate at the inner surface of the hole by isotropic etching to increase the width of the hole ;

using the insulating film having the opening as a mask, selectively plating a metal layer on the inner surface of the hole by electroless plating;

selectively removing a portion of the insulating film contacting the electroless-plated metal layer ;

selectively sputtering a metal layer on the insulating film and on the electroless-plated metal layer ; and

electroplating a low resistance metal layer on the electroless-plated metal layer and on the sputtered

metal layer using the electroless-plated metal layer and the sputtered metal layer as feeding layers.

32. The method of claim 31 wherein said hole has a depth and an aperture width in an aspect ratio (depth/aperture width) larger than 5/3.

33. The method of claim 31 wherein said electroless-plated metal layer is an Ni base alloy layer.

34. The method of claim 31 wherein said electroless-plated metal layer is formed by electroless-plating an Ni base alloy layer on the inner surface of the hole using a Pd layer selectively vapor-deposited at the bottom of the hole as a catalyst.

35. The method of claim 31 wherein said sputtered metal layer is formed by sputtering a first metal having a good adhesion to the surface of the substrate and to the surface of the electroless-plated metal layer and then sputtering a second metal having a low resistance on the sputtered first metal.

36. The method of claim 31 wherein said electroplated metal layer is an electroplated Au layer.

37. The method of claim 33 further including substituting the surface of the electroplated Ni base alloy layer by a substitution type electroless plating of Au.

38. The method of claim 34 further including substituting the surface of the electroplated Ni base alloy layer by a substitution type electroless plating of Au.

39. The method of claim 35 wherein the first metal is one selected from Ti, Cr, and Ni, and the second metal is Au.

40. The method of claim 31 further including:

after formation of the electroplated low resistance metal layer , polishing the rear surface of the substrate until the hole penetrates through the substrate ; and

forming a low resistance metal layer over the rear surface of the substrate, electrically contacting the electroplated metal layer .

41. A method of producing a via-hole in a semiconductor device, substantially as herein described with reference to Figure 1, Figures 2 and 3, Figures 4 and 5 or Figures 7 and 8 of the accompanying drawings.

42. In a semiconductor device, a via-hole substantially as herein described with reference to Figure 1, Figures 2 and 3, Figures 4 and 5 or Figures 7 and 8 of the accompanying drawings.

42. In a semiconductor device, a via-hole substantially as herein described with reference to Figure 1, Figures 2 and 3, Figures 4 and 5 or Figures 7 and 8 of the accompanying drawings.

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Databases (see below)
(i) UK Patent Office collections of GB, EP, WO and US patent specifications.

(ii) ONLINE: WPI

Documents considered relevant following a search in respect of Claims :-
1-42

Categories of documents

X: Document indicating lack of novelty or of inventive step.

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&: Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages	Relevant to claim(s)
A	EP 0388563 A1 (SGS)	

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